

Form PTO 1449 U.S. DEPARTMENT OF  
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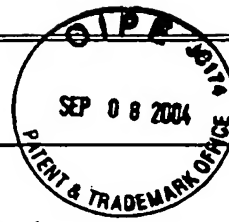
2343-182-27

APPLICANT

Robert B. REESE, et al.

SERIAL NO.

10/774,599



LIST OF REFERENCES CITED BY APPLICANT  
(Use Several Sheets if Necessary)

FILING DATE

February 10, 2004

GROUP ART UNIT

2124 2825

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO
	AK				
	AL				
	AM				

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

NMD	AN	Ivan E. Sutherland, "Micropipelines", Communications of the ACM, Vol. 32, No. 6, June 1989, pp. 720-738.
NMD	AO	D. E. Muller, et al., "A Theory of Asynchronous Circuits", Proc. Int. Symp. On Theory of Switching, Vol. 29, pp. 204-243 (1959).
NMD	AP	M. E. Dean, et al., "Efficient Self-Timing with Level-Encoded 2-Phase Dual-Rail (LEDR)", Advanced Research in VLSI (1991).
NMD	AQ	D. H. Linder, et al., "Phased Logic: Supporting the Synchronous Design Paradigm with Delay Insensitive Circuitry", IEEE Transactions on Computers, Vol. 45, No. 9, September 1996.
NMD	AR	F. Commoner, et al., "Marked Directed Graphs", J. Computer and Systems Sciences, Vol. 5, pp. 511-523 (1971).

EXAMINER

DATE CONSIDERED 01/18/06

\*EXAMINER: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.